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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/242,974	02/26/1999	MICHEL UGON	T2146-906088	1762

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MILES & STOCKBRIDGE PC
1751 PINNACLE DRIVE
SUITE 500
MCLEAN, VA 22102-3833

EXAMINER	
LI, AIMEE J	

ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 05/09/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/242,974	UGON, MICHEL	
	Examiner	Art Unit	
	Aimee J. Li	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 April 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *20-39 and 41-50* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *20-39 and 41-50* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 20-39 and 41-50 have been considered.

2. In response to the persuasive arguments presented in the After Final Request for Reconsideration filed 21 April 2005, the Examiner withdraws the Final Rejection mailed 16 November 2004.

Papers Submitted

3. It is hereby acknowledged that the following papers have been received and placed of record in the file:

Claim Rejections - 35 USC § 112

4. Claim 33 is rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. Claim 33 states "wherein the context of the main program is reestablished either automatically by the secondary program or automatically by the switching means before returning control to the main program" and is dependent on claim 32. Claim 32 states "wherein the secondary program does not modify general operating context of the main program in order to allow the main program to return without having the reestablish said context". Examiner was not able to locate enablement for the combination of these limitations. Specifically, the Examiner was unable to locate where the specification enables how to reestablish the operating context of the main program (Claim 33) when the context is not reestablished (Claim 32).

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 20-31, 34-37, 39, 41-50 are rejected under 35 U.S.C. 103(a) as being unpatentable over Anderson et al., U.S. Patent Number 5,613,114 (herein referred to as Anderson) in view of Griffin, III et al., U.S. Patent Number 5,249,294 (herein referred to as Griffin).

7. Referring to claim 20, Griffin has taught an unpredictable microprocessor or microcomputer comprising:

a. A main memory including an operating system, a main program, and a secondary program, wherein said secondary program is not related to the main program (Anderson column 3, lines 1-21 and 29-37 and Figure 1, elements 20, 60, 21, 22, and 23);

b. A first RAM-type working memory (Anderson column 3, lines 1-21; column 3, line 46 to column 4, line 6; and Figure 1, elements 31-33, 41-43, and 51-53);

c. A second RAM-type working memory (Anderson column 3, lines 1-21 and 46-64 and Figure 1, elements 31-33, 41-43, and 51-53);

d. A processor adapted to execute instructions from one or more of said main memory, said first working memory, and said second working memory (Anderson column 3, line 65 to column 4, line 5 and Figure 1, element 12);

e. A bus connecting the processor to the main memory, the first working memory and the second working memory (Anderson column 3, lines 16-17 and Figure 1, element 29);

f. Switching means for switching while the programs are running, from one of the two working memories to the other working memory while saving the contents of the two working memories (Anderson column 1, lines 16-43; column 2, lines 10-38; column 4, lines 15-31; and Figure 1), said switching means comprising:

i. Access registers associated with each of the main memory, the first working memory, and the second working memory (Anderson column 3, lines 1-21; column 3, line 46 to column 4, line 6; and Figure 1, elements 31-33, 41-43, and 51-53);

ii. At least one first block of registers that stores the operating context of the programs in the main memory (Anderson column 3, lines 1-21; column 3, line 46 to column 4, line 6; and Figure 1, elements 31-33, 41-43, and 51-53); and

iii. A switching circuit that enables one of the working memories and controls the access registers associated with each of the main memory, the first working memory and the second working memory (Anderson column 2, lines 10-38; column 5, lines 1-33; and Figure 1).

8. Anderson has not taught unpredictably jumping. Griffin has taught unpredictable jumping (Griffin columns 1-2, lines 58-11). In regards to Griffin, the interrupts are inherent in order to jump to the interim routines in the middle of a process. A person of ordinary skill in the

art at the time the invention was made would have recognized, and as supported by Griffin, that incorporating the means for de-correlating would prevent "clocks attacks" from compromising the system (Griffin Abstract, lines 1-8). Therefore, it would have been obvious at the time this invention was made to incorporate means for de-correlating as taught by Griffin in the device of Anderson to improve security.

9. Referring to claim 21, Anderson has taught the microprocessor or microcomputer further comprising a second block of registers for storing the operating context of the secondary program (Anderson column 3, lines 1-21; column 3, line 46 to column 4, line 6; and Figure 1, elements 31-33, 41-43, and 51-53).

10. Referring to claim 22, Anderson has not taught the microprocessor further including means for de-correlating the running of the programs from an isochronous clock. Griffin has taught means for de-correlating the running of the programs from an isochronous clock (Griffin columns 1-2, lines 36-2). A person of ordinary skill in the art at the time the invention was made would have recognized, and as supported by Griffin, that incorporating the means for de-correlating would prevent "clocks attacks" from compromising the system (Griffin Abstract, lines 1-8). Therefore, it would have been obvious at the time this invention was made to incorporate means for de-correlating as taught by Griffin in the device of Anderson to improve security.

11. Referring to claim 23, Anderson has taught wherein the main program can enable or inhibit the switching means by loading the switching circuit to switch and enable the working memories and the first block and second block of storage registers associated with each respective working memory, and storing, respectively, the operating context of the programs in

the main memory and the operating context of the secondary program (Anderson column 2, lines 10-38; column 5, lines 1-33; and Figure 1).

12. Referring to claim 24, Anderson has taught wherein the second working memory and its access registers are substituted for the first working memory and its access registers in utilization by a main program (Anderson column 2, lines 10-38; column 5, lines 1-33; and Figure 1).

13. Referring to claim 25, Anderson has not taught wherein the de-correlating means comprise a random number generator for triggering, via an interrupt circuit, the random interrupt for descynchronizing the running of the programs in the processor, by randomly jumping to the secondary program. Griffin has taught the de-correlating means comprise a random number generator for triggering, via an interrupt circuit, the random interrupt for descynchronizing the running of the programs in the processor, by randomly jumping to the secondary program (Griffin columns 1-2, lines 58-11). In regards to Griffin, the random number generator is inherent in order to determine the random duration interval and the interrupt circuit and interrupt are inherent in order to jump to the interim routines in the middle of a process. A person of ordinary skill in the art at the time the invention was made would have recognized, and as supported in Griffin, that incorporating the means for de-correlating would prevent "clocks attacks" from compromising the system (Griffin Abstract, lines 1-8). Therefore, it would have been obvious at the time this invention was made to incorporate means for de-correlating as taught by Griffin in the device of Anderson to improve security.

14. Referring to claim 26, Anderson has not taught means for de-correlating the running of the programs from an isochronous clock, wherein the de-correlating means comprises a time counting system independent from the processor that, after the time count, triggers an interrupt

for returning from the secondary program to the main program. Griffin has taught means for de-correlating the running of the programs from an isochronous clock, characterized in that the de-correlating means comprise a time counting system independent from the processor for, after the time count, triggering an interrupt for returning from the secondary program to the main program (Griffin columns 1-2, lines 58-11). In regards to Griffin, the clock system is inherent to determine the end of the random duration of the interim routine and triggering the interrupt is inherent to return to the predetermined process. A person of ordinary skill in the art at the time the invention was made would have recognized that incorporating the means for de-correlating as taught by Griffin provides a way to return to the main program to complete the processor's task. Therefore, it would have been obvious at the time this invention was made to incorporate means for de-correlating as taught by Griffin in the device of Anderson to be able to return to the main program.

15. Referring to claim 27, Anderson has not taught means for de-correlating the running of the programs from an isochronous clock, wherein the switching means is controlled by the processor and its program, by de-correlating means, by a timer, or by any combination of at least two of the three named elements. Griffin has taught means for de-correlating the running of the programs from an isochronous clock, characterized in that the switching means is controlled by the processor and its program, by de-correlating means, by a timer, or by any combination of at least two of the three named elements (Griffin columns 1-2, lines 58-11). In regards to Griffin, the clock system is inherent to determine the end of the random duration of the interim routine and triggering the interrupt is inherent to return to the predetermined process. A person of ordinary skill in the art at the time the invention was made would have recognized that

incorporating the means for de-correlating as taught by Griffin provides a way to return to the main program to complete the processor's task. Therefore, it would have been obvious at the time this invention was made to incorporate means for de-correlating as taught by Griffin in the device of Anderson to be able to return to the main program.

16. Referring to claim 28, Anderson has taught wherein the switching means is enabled by being loaded by the processor running a sequence in the main program sequence (Anderson column 2, lines 10-38; column 5, lines 1-33; and Figure 1).

17. Referring to claim 29, Anderson has taught wherein the secondary program uses a working space identical to that of the main program in the main memory (Anderson column 3, lines 29-45).

18. Referring to claim 30, Anderson has taught wherein the secondary program uses a working space smaller than that of the main program (Anderson column 3, lines 29-45).

19. Referring to claim 31, Anderson has taught wherein the switching means carry out the substitution of the memories and the associated contexts within the execution cycle of the instruction from the microprocessor (Anderson column 2, lines 10-38; column 5, lines 1-33; and Figure 1).

20. Referring to claim 34, Anderson has taught means for substituting the memory of the secondary program for the memory of the main program (Anderson column 3, lines 1-21; column 3, line 46 to column 4, line 6; and Figure 1, elements 31-33, 41-43, and 51-53).

21. Referring to claim 35, Anderson has taught wherein the main program can use the first working memory and the second working memory alternately or simultaneously (Anderson

column 3, lines 1-21; column 3, line 46 to column 4, line 6; and Figure 1, elements 31-33, 41-43, and 51-53).

22. Referring to claim 36, Anderson has taught wherein loading of the switching circuit makes it possible to mask or unmask de-correlating interrupts (Anderson column 5, lines 42-67; column 7, lines 27-50; and column 8, lines 20-27). In regards to Anderson, it is inherent to mask and unmask interrupts, since the switching means needs to be able to identify and use interrupts when they occur, randomly or not.

23. Referring to claim 37, Anderson has taught wherein an interrupt triggered by the secondary program effects return to the main program after the switching register has been properly loaded, by executing an instruction of the main program or the secondary program, in order to unmask the interrupts (Anderson column 2, lines 10-38; column 5, lines 1-33; and Figure 1).

24. Referring to claim 39, Anderson has not taught the microprocessor further including means of de-correlating the run-through of the programs with respect to an isochronal clock. Griffin has taught means of de-correlating the run-through of the programs with respect to an isochronal clock (Griffin columns 1-2, lines 36-2). A person of ordinary skill in the art at the time the invention was made would have recognized, and as supported by Griffin, that incorporating the means for de-correlating would prevent "clocks attacks" from compromising the system (Griffin Abstract, lines 1-8). Therefore, it would have been obvious at the time this invention was made to incorporate means for de-correlating as taught by Griffin in the device of Anderson to improve security.

25. Referring to claim 41, Anderson has taught wherein the second working memory and the associated access registers of the second working memory are adapted to be replaced in the use thereof by a main program, with said first memory and the associated access registers of the first memory (Anderson column 2, lines 10-38; column 5, lines 1-33; and Figure 1).

26. Referring to claim 42, Anderson has not taught wherein the de-correlating means comprise a random generator. Griffin has taught the de-correlating means comprise a random generator (Griffin columns 1-2, lines 58-2). A person of ordinary skill in the art at the time the invention was made would have recognized, and as supported by Griffin, that incorporating the means for de-correlating would prevent "clocks attacks" from compromising the system (Griffin Abstract, lines 1-8). Therefore, it would have been obvious at the time this invention was made to incorporate means for de-correlating as taught by Griffin in the device of Anderson to improve security.

27. Referring to claim 43, Anderson has not taught wherein the de-correlating means comprise a time counting system independent from the processor for enabling, at the end of a time count, an interruption trigger to return from the secondary program to the main program. Griffin has taught the de-correlating means comprise a time counting system independent from the processor for enabling, at the end of a time count, an interruption trigger to return from the secondary program to the main program (Griffin columns 1-2, lines 58-11). In regards to Griffin, the counting system is inherent to determine the end of the random duration of the interim routine and triggering the interrupt is inherent to return to the predetermine process. A person of ordinary skill in the art at the time the invention was made would have recognized that incorporating the means for de-correlating provides a way to return to the main program to

complete the processor's task. Therefore, it would have been obvious at the time this invention was made to incorporate means for de-correlating as taught by Griffin in the device of Anderson to be able to return to the main program.

28. Referring to claim 44, Anderson has taught wherein the switching means is controlled, either by one of the microprocessors and the program thereof, the random interruption system, a time counter, or a combination of at least two out of the three named elements (Anderson column 2, lines 10-38; column 5, lines 1-33; and Figure 1).

29. Referring to claim 45, Anderson has taught wherein the main program is adapted to enable or inhibit the switching means by loading the switching circuit of working memories and of the memorization register blocks associated with each respective working memory (Anderson column 2, lines 10-38; column 5, lines 1-33; and Figure 1).

30. Referring to claim 46, Anderson has taught wherein the second working memory and the associated access registers of the second working memory are adapted to be replaced in the use thereof by the main program, with said first working memory and the associated access registers of the first working memory (Anderson column 2, lines 10-38; column 5, lines 1-33; and Figure 1).

31. Referring to claim 47, Anderson has taught wherein the switching means is controlled, either by one of the microprocessors and the program thereof, the random interruption system, a time counter, or by a combination of at least two out of the three named elements (Anderson column 2, lines 10-38; column 5, lines 1-33; and Figure 1).

32. Referring to claim 48, Anderson has not taught wherein the interrupt circuit triggers the random number generator to thereby trigger the random interrupt to desynchronize execution of

the programs in the processor, by random connection to the secondary program. Griffin has taught the interrupt circuit triggers the random number generator to thereby trigger the random interrupt to desynchronize execution of the programs in the processor, by random connection to the secondary program (Griffin columns 1-2, lines 36-2). A person of ordinary skill in the art at the time the invention was made, as supported by Griffin, would have recognized that incorporating the interruption circuit prevents "clocks attacks" from compromising the system (Griffin Abstract, lines 1-8). Therefore, it would have been obvious at the time this invention was made to incorporate interruption circuit as taught by Griffin in the device of Anderson to improve security.

33. Referring to claim 49, Anderson has taught the switching means is controlled by one of the microprocessors and the program thereof, the random interruption system, a time counter or by a combination of at least two of the three named elements (Anderson column 2, lines 10-38; column 5, lines 1-33; and Figure 1). It is inherent that an interrupt can only occur when an interrupt is introduced by a source. Anderson has not taught the de-correlating means comprise a time counting system independent from the processor for enabling, at the end of a time count, the triggering an interruption to return from the secondary program to the main program. Griffin has taught the de-correlating means include a time counting system independent from the processor for enabling, at the end of a time count, the triggering of the random interrupt to return from the secondary program to the main program (Griffin columns 1-2, lines 58-11). In regards to Griffin, the counting system is inherent to determine the end of the random duration of the interim routine and triggering the interrupt is inherent to return to the predetermine process. A person of ordinary skill in the art at the time the invention was made would have recognized that

incorporating the means for de-correlating provides a way to return to the main program to complete the processor's task. Therefore, it would have been obvious at the time this invention was made to incorporate means for de-correlating as taught by Griffin in the device of Anderson to be able to return to the main program.

34. Referring to claim 50, Anderson has taught wherein the switching means is confirmed by loading from the processor executing a main program sequence (Anderson column 2, lines 10-38; column 5, lines 1-33; and Figure 1).

35. Claim 38 is rejected under 35 U.S.C. 103(a) as being unpatentable over Anderson in view in view of Griffin, as applied to claim 20 above, and further in view of Takagi, U.S. Patent Number 5,280,618 (herein referred to as Takagi). Anderson has not taught wherein the microcomputer or microprocessor is embodied in a monolithic integrated circuit. Takagi has taught the microcomputer or microprocessor is embodied in a monolithic integrated circuit (Takagi column 1, 14-22). A person of ordinary skill in the art at the time the invention was made would have recognized that incorporating the monolithic integrated circuit of Takagi broadens the number of applications the computer or processor may be used for. Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the monolithic integrated circuit of Takagi in the device of Anderson to increase usefulness.

36. Claims 32-33 are rejected under 35 U.S.C. 103(a) as being unpatentable over Anderson in view of Griffin as applied to claim 20 above, and further in view of Sakamura, U.S. Patent Number 5,029,069 (herein referred to as Sakamura).

37. Referring to claim 32, Anderson has not taught wherein the secondary program does not modify general operating context of the main program in order to allow the main program to return without having the reestablish said context. Sakamura has taught wherein the secondary program does not modify general operating context of the main program in order to allow the main program to return without having the reestablish said context (Sakamura column 178, lines 55-59). A person of ordinary skill in the art at the time the invention was made would have recognized that not saving the context and having to reestablish the context of unmodified areas reduces the number of wasted cycles and decreases the time required for a context switch (Sakamura column 178, lines 55-59), thereby increasing the speed and efficiency of the device. Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the context saving of Sakamura in the device of Anderson to increase processor speed and efficiency.

38. Referring to claim 33, Anderson has taught wherein the context of the main program is reestablished either automatically by the secondary program or automatically by the switching means before returning control to the main program (Anderson column 2, lines 10-38; column 5, lines 1-33; and Figure 1).

Response to Arguments

39. Applicant's arguments, see After Final Amendment, filed 21 April 2005, with respect to the rejection(s) of all claim(s) under Okin in view of Fletcher and in further view of Griffin have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of the above rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Aimee J. Li whose telephone number is (571) 272-4169. The examiner can normally be reached on M-T 7:30am-5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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5 May 2005

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